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EXAMINER

WARREN, MATTHEW E

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2815

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/594,091

Applicant(s)

ITOH

Examiner

Matthew E. Warren

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This Office Action is in response to the Amendment filed on May 17, 2002.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Semiconductor Memory Device Having Planarized Upper Surface and a SiON Moisture Barrier."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 3, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Arita et al. (US 6,046,490).

Arita shows (fig. 1) a semiconductor device comprising a transistor having a first and second impurity region (3) formed in a substrate (1), and a gate electrode (5). A first insulating layer (6) covers the transistor. A capacitor (10) is formed on the insulating layer, the capacitor having a dielectric (8) formed of a high dielectric constant material (col. 8, lines 39-45), and an upper electrode (9) and lower electrode (7) with the

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dielectric positioned therebetween. A silicon oxide film (22) is formed over the capacitor and has its upper surface planarized. A silicon nitride oxide film (14) is formed on the oxide to prevent moisture from penetrating the device (col. 6, lines 10-17). A second insulating film (15) is formed between the capacitor and the silicon oxide film.

With respect to the limitation of the "nitrogen being introduced all over the planarized surface of the silicon oxide film," a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, **190 USPQ 15 at 17**(footnote 3). See also *in re Brown*, **173 USPQ 685**; *In re Luck*, **177 USPQ 523**; *In re Fessmann*, **180 USPQ 324**; *In re Avery*, **186 USPQ 116** *in re Wertheim*, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and *In re Marosi et al*, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita et al. (US 6,046,490) as applied to claim 1 above, and further in view of Singh et al. (US 5,847,464).

Arita shows of the element of the claims except the cavities formed in the silicon oxide film. Singh et al. discloses a semiconductor device comprising an interlevel dielectric layer (46) which has cavities (voids 72, 74, etc) formed throughout the layer (see fig. 3b). The cavities help lower the capacitance and ultimately helps reduce RC delay of signals along adjacent metal lines (col. 5 lines 57-67, col. 6, lines 48-64). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor capacitor of Arita by forming cavities in the silicon oxide layer as taught by Singh to reduce capacitance and lower delay of signals along metal signal lines.

Claims 5, and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al. (US 5,990,507) in view of Arita et al. (US 6,046,490).

Mochizuki et al. shows (fig. 17) a semiconductor device comprising a transistor having a first and second impurity region (S, D) formed in a substrate (1), and a gate

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electrode (G, 4 & 5). A first insulating layer (10) covers the transistor. A capacitor is formed on the insulating layer, the capacitor having a dielectric (18) formed of a ferroelectric material, and an upper electrode (19) and lower electrode (17) with the dielectric positioned therebetween. A second insulating film (13) is formed on the capacitor. A local interconnection (22) is formed on the second insulating film for connecting the upper electrode of the capacitor to the first impurity region (S). Third insulating film (30) is formed on the local interconnection and the second insulating film. A first wiring (BL) is formed on the third insulating film and electrically connects to the second impurity region (D) via a hole which is formed in the first, second, and third insulating films. A fourth insulating film (39) is formed on the first wiring and has a planarized upper surface. The upper surface of the first insulating film is planarized. A second wiring is formed on the fourth film and connects to the first wiring via a hole formed through the fourth insulating layer (col. 24, lines 49-67). Mochizuki shows all of the elements of the claims except the third and fourth insulating films formed specifically of silicon oxide. Arita shows (fig. 1) a semiconductor device comprising a transistor having a capacitor device covered by third and fourth insulating films, which are formed of silicon oxide (col. 6, lines 1-17). A silicon nitride oxide film (14) is formed on the oxide. With this configuration, moisture is prevented from penetrating the device (col. 6, lines 10-17). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating layers Mochizuki by forming oxide and then oxynitride as taught by Arita to prevent moisture from penetrating the device.

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With respect to the limitation of the "nitrogen being introduced all over the planarized surface of the silicon oxide film," a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, **190 USPQ 15 at 17**(footnote 3). See also *in re Brown*, **173 USPQ 685**; *In re Luck*, **177 USPQ 523**; *In re Fessmann*, **180 USPQ 324**; *In re Avery*, **186 USPQ 116** *in re Wertheim*, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and *In re Marosi et al*, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al. (US 5,990,507) in view of Arita et al. (US 6,046,490), as applied to claim 5 above, and further in view of Singh et al. (US 5,847,464).

Mochizuki and Arita show all of the elements of the claims except the cavities exposed from an upper surface of the insulating film. Singh et al. shows (fig. 5 a-c)

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cavities (76, 78, 76", 78") in an upper insulating film (46) which are partially exposed from the film. Another insulating film (80) is formed on the first insulating (46) film to cover the cavities. The cavities help lower the capacitance and ultimately helps reduce RC delay of signals along adjacent metal lines (col. 5 lines 57-67, col. 6, lines 48-64). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor capacitor of Mochizuki and Arita by forming cavities in the silicon oxide layer as taught by Singh to reduce capacitance and lower delay of signals along metal signal lines.

Response to Arguments

Applicant's arguments filed with respect to claims 1-12 have been fully considered but they are not persuasive. The applicant primarily asserts that the cited references do not show all of the elements of the claims, particularly the nitrogen introduced over the surface of an upper layer of silicon oxide. As stated in the above rejection, the added limitation of the nitrogen being introduced on the surface of the oxide is a product by process limitation. The applicant further states that introduction of nitrogen by a plasma process subsequently forms SiON and thusly prevents moisture from entering the device (page 23, lines 4-19). Arita also discloses that a SiN or SiON film is formed as a passivation layer over the device to prevent moisture from entering (col. 6, lines 10-18). Arita also uses the same process of plasma annealing in a nitrogen gas to form the SiON layer (col. 4, lines 31-36 and col. 6, lines 30-35). In this way,

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nitrogen is introduced on the surface of the lower oxide film. For these reasons, the cited references show all of the elements of the claims and this Action is made final.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Morozumi et al. (US 6,246,105 B1) also shows an upper passivation layer of nitride for moisture prevention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW

MEW
July 29, 2002



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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